Abstract of the Disclosure

An integrated circuit having a MOS structure with reduced parasitic bipolar transistor action. In one embodiment, a MOS integrated circuit device comprises a substrate having a working surface, at least one body region and for each body region a source and a layer of narrow band gap material. Each body region is formed in the substrate proximate the working surface of the substrate. Each layer of narrow band gap material is positioned in a portion of its associated body region and proximate the working surface of the substrate. Each layer of narrow band gap material has a band gap that is narrower than the band gap of the substrate in which each of the body regions are formed. Each source region is formed in an associated body region. At least a portion of each source region is also formed in an associated layer of narrow band gap material.